REMARKS/ARGUMENTS

Claims 1-6, 8, 11-17 and 20 are currently pending. Applicants have amended claims 1 and 12. Applicants submit that no new matter has been added to the application as result of these amendments.

Claims 1-6, 8, 11-17 and 20 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,995,736 to Aleksic et al. (hereinafter "Aleksic").

Claim 7 stands rejected under 35 U.S.C. §103(a) as being obvious over Aleksic in view of U.S. Patent Application Publication No. 2005/0114818 to Khakzaki et al. (hereinafter "Khakzaki").

Claims 10 and 19 stand rejected under 35 U.S.C. §103(a) as being obvious over Aleksic in view of U.S. Patent No. 6,536,017 to Sanders (hereinafter "Sanders").

Reconsideration in view of the amendments above and the remarks below is respectfully requested.

Rejections under 35 U.S.C. §102

Claims 1-6, 8, 11-17 and 20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Aleksic.

Applicants submit that Aleksic fails to anticipate claim 1 for at least the reasons provided. For example, claim 1 recites, in part, a computer program product for editing a file describing a circuit design so that the HDL code in the file is compatible with a new programmable logic integrated circuit (IC), the method comprising:

code for locating black box declarations and black box instances in the file;
code for gathering information about the black box declarations and instances, wherein a black box represents a circuit block within a circuit design and the information gathered represents one or more attributes of a circuit block represented by a black box;

code for editing the black box declarations to create equivalent black box declarations that are compatible with the new programmable logic IC using the information;

code for editing the black box instances to create equivalent black box instances that are compatible with the new programmable logic IC using the information;

code for generating a detailed report that indicates where the black box declarations and instances were found in the code and the equivalent declarations and instances that the black boxes were replaced with

Applicants submit that Aleksic fails to teach at least (1) code for locating black box declarations and black box instances in the HDL file, (2) code for gathering information about the black box declarations and instances; and (3) code for editing the black box declarations and instances.

Applicants submit that Aleksic is directed to an integrated circuit modeling system for facilitating automated design of register based hardware devices by generating major pieces of the development outputs from a single input, such as a single special register specification source file. The register specification file is a text file that contains all of the register information about the device being developed. The system uses a series of associated pre-stored modeling templates in different programming languages that access the register specification source file and automatically generate behavioral model register code and IC simulation code. Aleksic, Abstract.

Applicants submit that Aleksic fails to teach code for locating black box declarations and black box instances in the HDL file as recited in claim 1. The Office Action relies upon Fig. 2, reference no. 34, Fig. 3, reference no. 34, Fig. 5, reference no. 82, and Figs. 6A-6E to teach this feature of claim 1. However, the cited portions of Aleksic merely describe the model register generator (Fig. 2, reference no. 36) being used to generate a plurality of files, including behavioral model register C++ code (Figs. 6B and 6C) and hardware design register VHDL code (Figs. 6D and 6E) from the register specification file described above (Fig. 2, reference no. 34, Fig. 3, reference no. 34, and Fig. 6A). In the system described in Aleksic, if a user wishes to change the design of a register based hardware device, such as to be compatible with a different programmable IC, the user edits the register specification file, and the associated files including the VHDL code are regenerated from the register specification file by the model register generator. See Aleksic, col. 12, line 56 - col. 13, line 10.

In contrast, the computer program product recited in claim 1 advantageously facilitates conversion of HDL code describing a circuit design for a first programmable IC into HDL code compatible with a new programmable logic IC, including locating black box instances

and declarations in the HDL file, gathering information about those black box instances and declarations, and editing the black box instances and declarations to be compatible with the new IC. In Aleksic, a user must manually edit the register specification file in order to reconfigure the register based hardware device. Aleksic is silent as to locating black box instances and declarations in HDL files in order to convert the HDL to be compatible with a new programmable IC. Therefore, Aleksic fails to teach this feature of claim 1.

Applicants submit that Aleksic also fails to teach code for gathering information about the black box declarations and instances as recited in claim 1. The Office Action relies upon the model register file and col. 3, lines 53-67, col. 4, lines 1-17, col. 6, lines 15-67, and col. 8 lines 8-24 of Aleksic to teach this feature of claim 1. However, as described above, in Aleksic, the register information in the model register file is used to generate a plurality of files including the VHDL files (Fig. 2, reference no. 38, and Figs. 6D and 6E). Aleksic is silent as to gathering information about the black box definitions in the HDL code. Therefore, Aleksic also fails to teach this feature of claim 1.

Applicants further submit that Aleksic fails to teach "code for editing the black box declarations to create equivalent black box declarations that are compatible with the new programmable logic IC using the information" gathered about the black box declarations and "code for editing the black box instances to create equivalent black box instances that are compatible with the new programmable logic IC using the information" gathered about the black box declarations as recited in claim1. The Office Action relies upon col. 8 of Aleksic to teach this feature of claim 1. However, the cited portions of Aleksic merely describe editing the register model file, and regenerating the behavioral simulation content in C/C++ (Fig. 2, reference no. 40, and Figs. 6B and 6C) and hardware simulation models in VHDL (Fig. 2, reference no. 38, and Figs. 6D and 6E) from the modified register specification file. As described above, Aleksic is silent as to locating and gathering information about the black box instances and declarations in the HDL file. Aleksic is similarly silent as to editing the black box instances and declarations in the HDL file to create equivalent black box instances and declarations that are compatible with a new programmable logic IC. Changes to the design of the design of register based hardware device in Aleksic are accomplished by editing the model

register file. See Aleksic, col. 3, line 53 - col. 4, line 3. Therefore, Aleksic also fails to teach this feature of claim 1.

Applicants further submit that Aleksic also fails to teach code for generating a detailed report that indicates where the black box declarations and instances were found in the code and the equivalent declarations and instances with which the black boxes were replaced as recited in claim 1. The Office Action relies upon Fig. 5 of Aleksic to teach this feature of claim 1. However, Aleksic merely describes generating a report that highlights the differences between the current and previous versions of the model register file. See Aleksic, col. 8, lines 48-60. The report described in Aleksic does not indicate where the black box declarations and instances were found in the HDL code and the equivalent declarations and instances in the HDL code with which the black box declarations and instances were replaced as recited in claim 1. The report described in claim 1 advantageously provides a user with an indication as to which black box declarations and instances in the HDL code were modified in order to convert the HDL code to be compatible with the new programmable IC device. Therefore, Aleksic also fails to teach this feature of claim 1.

Therefore, for at least the reasons provided, Applicants submit that Aleksic fails to anticipate claim 1. Claim 12 should be allowable for similar reasons as claim 1. Furthermore, the dependent claims 2-6, 8 and 11, which depend from claim 1, and dependent claims 13-17 and 20, which depend from claim 12, should also be in condition for allowance at least due to their dependence from claims 1 and 12, respectively.

Accordingly, Applicants respectfully request that the rejection of claims 1-6, 8, 11-17 and 20 under 35 U.S.C. 102(b) be withdrawn.

Rejections under 35 U.S.C. §103

Claim 7

Claim 7 stands rejected under 35 U.S.C. §103(a) as being obvious over Aleksic in view of Khakzaki.

Claim 7 depends from claim 1, and the rejection of claim 7 is premised on the assertion that Aleksic discloses the features recited in claim 1 and Khakzaki discloses or suggests

the remaining features of claim 7. As discussed above, however, Aleksic does not disclose or suggest all of the features recited in claim 1. As best understood, Khakzaki provides no teaching or suggestion that would remedy this deficiency. Therefore, the rejection is based on a flawed premise and cannot be maintained. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 7.

Claims 10 and 19

Claims 10 and 19 stand rejected under 35 U.S.C. §103(a) as being obvious over Aleksic in view of Sanders.

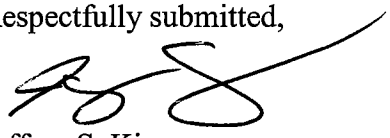
Claims 10 depends from claim 1, and claim 19 depends from claim 12. The rejection of claims 10 and 19 is premised on the assertion that Aleksic discloses the features recited in claims 1 and 12, and Sanders discloses or suggests the remaining features of claim 10 and 19. As discussed above, however, Aleksic does not disclose or suggest all of the features recited in claims 1 and 12. As best understood, Sanders provides no teaching or suggestion that would remedy this deficiency. Therefore, the rejection is based on a flawed premise and cannot be maintained. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 10 and 19.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 858-350-6100.

Respectfully submitted,



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